Docket No. 210067US2

#16
1800
H6-03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Hidemasa ZAMA, et al.

SERIAL NO: 09/883,959 GAU: 2819

FILED: June 20, 2001 EXAMINER: TAN, V.

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT, LOGIC OPERATION CIRCUIT, AND FLIP FLOP

REQUEST FOR EXTENSION OF TIME UNDER 37 C.F.R. 1.136

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

It is hereby requested that a **two and three** month extension of times be granted to January 1, 2003 for

☐ filing a response to the Official Action dated:

☐ responding to the requirements in the Notice of Allowability dated:

☐ filing the Formal Drawings. The Issue Fee due has been timely filed.

☐ responding to the Notice to File Missing Parts of Application dated:

■ filing a Notice of Appeal. A timely response to the final rejection, due October 1, 2002 has been filed.

filing an Appeal Brief. A Notice of Appeal was filed on:

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee amount shown below is reduced by one-half.

The required fee of $820.00 is enclosed herewith by check and any further charges may be made against the Attorney of Record's Deposit Account No. **15-0030**. A duplicate copy of this sheet is enclosed.

Respectfully Submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Registration No. 25, 599

W. Todd Baker
Registration No. 45,265

Eckhard H. Kuesters
Registration No. 28,870

22850
Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 10/01)
I:\ATTY\WTB\210067US\EOT 2 JAN 03.DOC

01/03/2003 JADD01 00000014 09883959
01 FC:1253 820.00 OP